

reject claim 1, the Examiner has effectively replaced the adhesive layer 5 of APA with the alleged adhesive layer 8 of Amagai in order to read on the limitations of claim 1. As such, the adhesive layer 5 of APA does not exist in the proposed combination, but rather, the alleged adhesive layer 8 of Amagai has replaced the layer 5 of APA. It is submitted that the Examiner can not rely on APA to disclose the limitation of claim 5 while at the same time relying on Amagai to disclose the limitation of claim 1 with respect to the same adhesive layer recited in the claims.

Claim 5 effectively recites two size restrictions on the same adhesive layer, whereas the Examiner has relied on the separate size restrictions of two different adhesive layers taught in the prior art as if they were one. Accordingly, the device resulting from the Examiner's proposed combination does not have an adhesive layer which is "smaller in size than the primary surface of said circuit board" as recited in claim 5. Instead, the proposed combination results in the device of APA having the alleged adhesive layer 8 of Amagai, which is NOT smaller in size than the alleged circuit board 3. That is, the proposed combination would result in the adhesive layer 5 of APA being the same size as the circuit board 1 as taught by Amagai.

The cited prior art does not disclose or suggest the *combination* of an adhesive layer which is *both* "greater in size than the primary surface of said semiconductor element" as recited in claim 1 *and* "smaller in size than the primary surface of said circuit board" as recited in claim 5 (see Figures 1-3 for exemplary embodiments, where the adhesive layer 5 is bigger than the semiconductor element 10 but smaller than the circuit board 1). Neither APA nor Amagai, alone or in combination, discloses the combination of the two limitations recited in claims 1 and 5. It is respectfully submitted that the Examiner has improperly relied on APA for disclosing the size

of the adhesive layer for rejecting claim 5 while relying on Amagai to disclose a different size of the same adhesive layer for rejecting claim 1.

However, the cited prior art suggests only one of the two distinct sizes taught by APA and Amagai for the adhesive layer, and does not suggest a "middle" size for the adhesive layer between the two sizes as recited in claim 5 in combination with claim 1. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that APA and Amagai "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no objective reason on the record to combine the teachings of the cited prior art in the manner set forth by the Examiner. As discussed above, neither APA nor Amagai disclose or suggest an adhesive layer having a "middle" size which is larger than the semiconductor element but smaller than the circuit board.

At best, the Examiner has attempted to show only that the elements of the claimed invention are *individually* known (i.e., adhesive layer which is larger than semiconductor element OR adhesive layer smaller than circuit board) without providing a *prima facie* showing of obviousness that the *combination* of elements (i.e., adhesive layer which is larger than semiconductor element AND adhesive layer smaller than circuit board) recited in claim 1 in

combination with claim 5, is known or suggested in the art. It is respectfully submitted that the Examiner has selected bits and pieces of the cited prior art and relied solely on improper hindsight reasoning using only Applicants' specification as a guide to reconstruct the claimed invention.

Based on all the foregoing, it is submitted that claim 5 is patentable over APA in view of Amagai and Jiang et al.. Accordingly, it is respectfully requested that the rejection of claim 5 under 35 U.S.C. § 103 over APA in view of Amagai and Jiang et al., be withdrawn.

B. CLAIM 1-3

In response to Applicants' arguments that Amagai does not provide any motivation for using a wider adhesive, the Examiner alleges that one of ordinary skill in the art would have found that "such bonding layer being greater in size than the element would provide improved adhesion and rigidity for the APA's package." This allegation is respectfully traversed. The Examiner has not provided any *objective* evidence *from the prior art* as to why having an adhesive layer greater in size than the semiconductor element would improve adhesion/rigidity. The adhesive layer 5 of APA is designed simply to adhere the semiconductor element 10 to the circuit board 1. Increasing the size of the adhesive layer 5 beyond the size of the semiconductor element 10 would not meaningfully improve the adhesion between the semiconductor element 10 and the circuit board 1 *because the amount of surface contact between the semiconductor element 10 and adhesive layer 5 would still be the same.*

It is respectfully submitted that the Examiner's alleged motivation is derived solely from Applicants' specification and is therefore improper hindsight reasoning. For example, page 6, lines 5-11 and/or page 8, lines 24-28 describe how the area covered by the adhesive layer beyond the semiconductor element absorbs stress due to a difference in thermal expansion coefficients so

that the stress exerted on the solder joints 31-32 is alleviated. Further, on page 8, Applicants disclose that because of the larger adhesive layer, "the point about which the circuit board 1 is to warp is distant from the external electrodes provided on outermost periphery of the semiconductor device" so as to alleviate the stress exerted on the solder joints 31-32, thereby improving reliability and rigidity of the device.

These technically based findings (e.g., differences in thermal expansion coefficients and warping location of circuit board) are the only evidence on the record for supporting the motivation of providing the adhesive layer having a greater size than the semiconductor element. The cited prior art does not acknowledge nor consider such findings, and there is no objective evidence on the record that the prior art suggests the desirability of having a larger adhesive layer. Again, at best, the Examiner has attempted to show only that the elements of the claimed invention are *individually* known without providing a *prima facie* showing of obviousness that the *combination* of elements recited in claim 1 is known or suggested in the art. It is respectfully submitted that the Examiner has selected bits and pieces of the cited prior art and relied solely on improper hindsight reasoning using only Applicants' specification as a guide to reconstruct the claimed invention.

If the Examiner maintains the pending rejection, it is respectfully requested that he provide some *objective* technical evidence *from the prior art* (i.e., independent of Applicants' specification) that supports his allegation that the motivation for modifying APA with Amagai is suggested by the prior art rather than Applicants' specification.

Furthermore, it is submitted that the present invention provides new and unexpected results over the device of the proposed combination of references. As such, it is submitted that the proposed combination would not have been obvious to one of ordinary skill in the art (absent

hindsight reasoning) because the claimed invention improves upon known devices by correcting a problem previously undealt with in the prior art. That is, the *combination* of elements recited in claims 1-3, even assuming *arguendo* they are known *individually* in the art, provide certain advantages and benefits as a combination that are both new and unexpected over existing devices.

Accordingly, it is submitted that these differences between the prior art and the present invention emphasize the non-obviousness of the *combination* of elements recited in claims 1-3, so as to effectively render the proposed combination of APA, Amagai and Jiang et al. improper. Specifically, none of the cited prior art recognizes or attempts to solve the interface problem between the adhesive layer and molding resin which leads to undesirable moisture absorption and high temperature deterioration.

In particular, when the adhesive layer extends up to the periphery of the substrate as in the proposed combination set forth by the Examiner (i.e., where the APA adhesive layer is replaced with the Amagai adhesive layer), the interface between the adhesive layer and the molding resin may tend to tear, and moisture absorption or high temperature deterioration might be caused. In contrast, in the present invention, the peripheral region of the substrate can be covered by the molding resin *in combination* with an adhesive layer which is larger than the semiconductor element, so that the above characteristics are improved and the benefits of both features can be obtained in a single device. None of the cited prior art discloses or suggests such a combination, let alone recognize or appreciate the dual benefits derived therefrom. Accordingly, the present invention provides a device which is superior to known prior art devices, rendering any combination of references to reach such a construction as non-obvious. In general, an adhesive layer tends to absorb moisture more than a molding resin, i.e., Tg (glass transformation temperature) is low.

Additionally, in the proposed combination, the chip is provided via an elastmer layer on a flexible substrate, whereas in the present invention the chip can be provided on a rigid substrate so as to further improve the characteristics of the device.

Based on the foregoing, it is submitted that claim 1 and its dependent claims are patentable over APA in view of Amagai and Jiang et al.. Accordingly, it is respectfully requested that the rejection of claims 1-3 under 35 U.S.C. § 103 over APA in view of Amagai and Jiang et al., be withdrawn.

C. Claims 4 and 6

Claims 4 and 6 stand rejected under 35 U.S.C. § 103 over APA in view of Amagai, Jiang et al. and Lee et al.. This rejection is respectfully traversed for the following reasons. Even assuming *arguendo* proper, the proposed combination does not disclose or suggest each and every limitation of the claims.

For example, the Examiner relies on Lee for disclosing the limitation of claim 6, which recites "wherein said adhesive layer extends outside an outer edge of the primary surface of said semiconductor element ***without reaching an outer edge of the primary surface of said circuit board***" (emphasis added). In contrast, the alleged adhesive layer 29 of Lee et al. ***does reach*** the outer edge of the primary surface of the alleged circuit board 20, 28 (*see* Figure 4 of Lee et al.).

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 4 and 6 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Based on the foregoing, it is submitted that claims 4 and 6 are patentable based on their own merits, in addition to being dependent on novel claim 1.

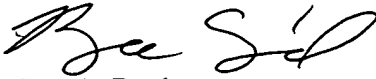
CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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